IN THE SPECIFICATION:

Please amend the paragraph beginning at page 1, line 14, as follows

The Peripheral Component Interconnect (PCI) specification (downloadable from www.pci-sig.com) defines how one or more peripheral devices can communicate with a computing device ~~}~~over a serial input/output bus link. The serial link can be within a single computing device or can link one or more computing devices and peripheral devices. The original PCI specification defines a 32-bit PCI bus that operates at 33 MHz with a peak throughput of 132 Megabytes/second. Until recently, the performance of the original PCI specification was adequate for most applications. As the processing rates of commercially available processors have increased, the processing capacity of the processors to process data eventually exceeded the capacity of the PCI bus to deliver data. Thus, recent processors can process data faster than the PCI bus can deliver the data to processor.

Please amend the paragraph beginning at page 6, line 1, as follows.

FIG. 4 is a schematic block diagram illustrating an exemplary charge pump 240 of FIG. 2 in further detail. As shown in FIG. 4, the charge pump 240 includes ~~four~~ two PMOS transistors 410, 430 and two NMOS transistor 420, 440 and two current sources 450, 460. The transistors 410, 430, 420, 440 are connected to the UP and DN control signals, respectively, generated by the amplitude control circuit 230 of FIG. 3. The up current source 450 is active when the UP control signal is enabled by the amplitude control circuit 230 (i.e., when Vcm < Vref1). When the up current source 450 is active, the charge pump 240 will change the voltage at out+/out- towards Vref2. Likewise, the down current source 460 is active when the DN control signal is enabled by the amplitude control circuit 230 (i.e., when Vcm > Vref2). When the down current source 460 is active, the charge pump 240 will change the voltage at out+/out- towards Vref1.